IPIC (Intelligent Power IC) High Side Solenoid Driver

HITACHI

ADE-207-207 (Z) 1st Edition July 1996

Description

The HA13705C is high side power driver IC with protectors and diagnostic function. The device is especially designed to switch inductive loads.

Functions

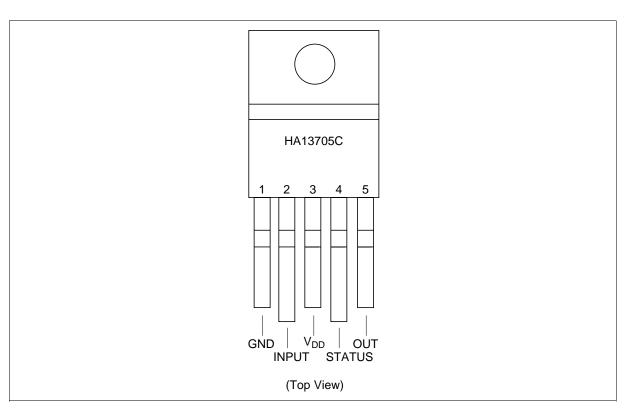
- Power MOS source follower output (2 A)
- With Over Voltage Shut Down circuit (OVSD)
- With Over Current protector circuit (OCSD)
- With Over Temperature Shut Down circuit (OTSD)
- With diagnostic circuit and status output
- With fail safe function under input open circuit condition
- With low voltage inhibit circuit (LVI)
- With output negative voltage clamp circuit

Features

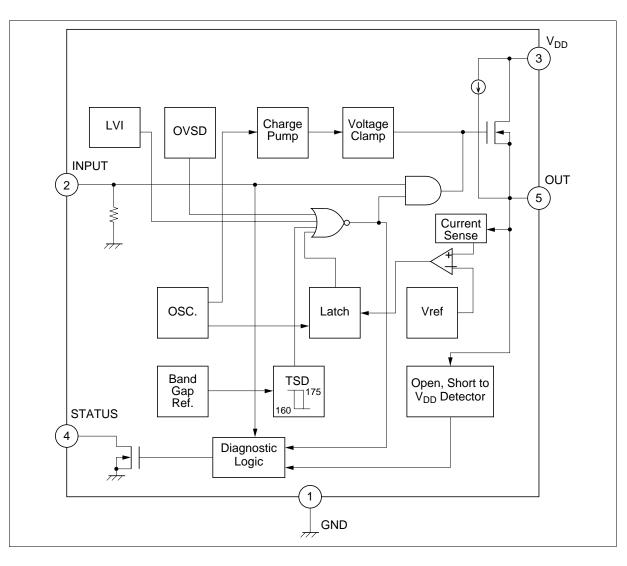
- Protected against 60 V load dump condition
- Low R_{ON} (0.17 Ω Typ)
- Wide operating supply voltage range $(V_{DD} = 7 \text{ V to } 25 \text{ V})$
- High sustaining voltage (-25 V)
- Protected against reverse supply voltage (-13 V)
- Protected against short circuit condition
- Input compatible with TTL, LS-TTL, or 5 V CMOS



Pin Arrangement



Block Diagram



Truth Table

| Mode | In | Out | Status | |
|--------------------------|----|-----|--------|--|
| Normal | L | L | L | |
| | Н | Н | Н | |
| Load short | L | L | L | |
| | Н | L | L | |
| Load open | L | Н | Н | |
| | Н | Н | Н | |
| Short to V _{DD} | L | Н | Н | |
| | Н | Н | Н | |
| OTSD *1 | L | L | L | |
| | Н | L | L | |
| OVSD *2 | L | L | Н | |
| | Н | L | Н | |
| LVI *3 | L | L | Н | |
| | Н | L | Н | |

L: Low level (0.8 V)
H: High level (2.0 V)

Notes: 1. OTSD: Over temperature shut down

2. OVSD: Over voltage shut down

3. LVI: Low voltage inhhibit

Absolute Maximum Ratings $(Ta = 25^{\circ}C)$

| Item | Symbol | Rating | Unit | Notes | |
|---|-----------------|------------------------|------|-------|--|
| Continuous supply voltage | V_{DD} | -13 to 35 | V | 1 | |
| Transient supply voltage | V _{DD} | 60 | V | 2 | |
| Input voltage | V_{IN} | -0.3 to 30 | V | | |
| Output voltage | Vout | –25 to V _{DD} | V | 3 | |
| Status voltage | Vs | -0.3 to +15 | V | | |
| Output current | lout | _ | Α | 3, 4 | |
| Status current | ls | 5 | mA | | |
| Power dissipation | P _T | _ | W | 5 | |
| Package thermal resistance/ Junction to case | θј–с | 5 | °C/W | | |
| Package thermal resistance/ Junction to air | θј–а | 70 | °C/W | | |
| Junction temperature range | Tj | -40 to 150 | °C | | |
| Storage temperature range | Tstg | -55 to +150 | °C | | |

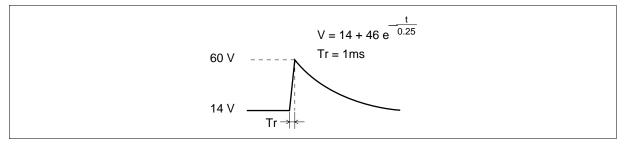
Notes: 1. Recommended operating voltage:

 $V_{DD} = 7 \text{ to } 16 \text{ V (Normal)}$

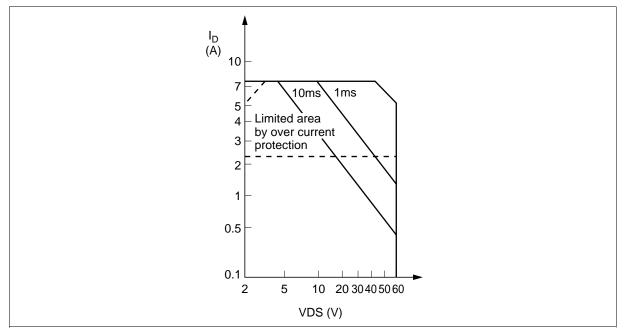
16 to 25 V (Jump up start 5 minutes MAX)

-13 V (Reverse Battely 5 minutes MAX)

2. Load dump condition



3. Output Transistor ASO (Reference Data)



- 4. Internally limited
- 5. Maximum power dissipation $(P_T (Max))$ can be defined as:

 P_T (Max) = (Tjopr(Max) – Tambient) / (θ j-c + θ c-a)

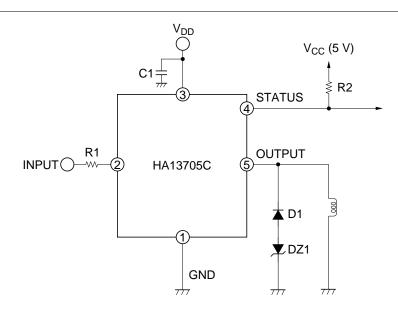
 θ c-a: Thermal resistance between case and air (Depend on heat sink size)

Electrical Characteristics (Ta = 25°C, V_{CC} = 12 V ±10%)

| Output R (ON) Ros(ON) Ros(ON) - 0.17 0.36 Ω I ₀ = 2 A (@Tj = -40 to 150°C) 5 Operating supply voltage range V _{DD} 7 - 25 V 3 Quiescent current I _{DD1} - - 0.3 mA V _{IN} = 0 V, Vout = 0 V 3 Output leakage current I _{LEAK} - - 0.1 mA V _{IN} = 5.5 V, Vout = 0 PC 3 Input threshold voltage V _{IL} - - 0.8 V - 2 Input current I _{IL} -10 - 60 μA V _{IN} = 0.8 V 2 Input current I _{IL} -10 - 60 μA V _{IN} = 0.8 V 2 Input current I _{IL} -10 - 60 μA V _{IN} = 0.8 V 2 Input current I _{IL} -10 - 50 μs I _I - 2,5 - - - < | Item | | Symbol | Min | Тур | Max | Unit | Test Conditions | Pin | Note |
|---|--------------------------|-------------|---------------------|------|------|------|------|--|------|------|
| Voltage range Quiescent current I _{DD1} — — — — — — — — — — — — — — — — — — — | Output R (ON) | | R _{DS(ON)} | _ | 0.17 | 0.36 | Ω | | 5 | |
| Output leakage current I _{LEAK} | | | V_{DD} | 7 | _ | 25 | V | | 3 | |
| Output leakage current I_LEAK — — 0.1 mA V _{DO} = 25 V, V _N = 0 V, V 5 Input threshold voltage V _{IL} — — 0.8 V 2 V _{IN} 2.0 — — V — 2 Input current I _{IL} —10 — 60 µA V _{IN} = 0.8 V 2 Propagation delay time I _{IL} —10 — 60 µA V _{IN} = 5.0 V 2 Propagation delay time t _{4(ON)} — — 50 µS I ₀ = 1 A 2,5 Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Tripe colspan="8">Input colspan="8">Tripe colspan= | Quiescer | nt current | I _{DD1} | _ | _ | 0.3 | mA | $V_{IN} = 0 \text{ V}, \text{ Vout} = 0 \text{ V}$ | 3 | |
| Input threshold voltage | | | I _{DD2} | _ | 6.0 | 10.0 | mA | $V_{IN} = 5.5 \text{ V}, \text{ Vout} = \text{open}$ | 3 | |
| Propagation delay time I I I I I I I I I | Output leakage current | | I _{LEAK} | _ | _ | 0.1 | mA | | 5 | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Input threshold voltage | | V _{IL} | _ | _ | 0.8 | V | | 2 | |
| The color of th | | | V _{IH} | 2.0 | _ | _ | V | | 2 | |
| Propagation delay time t _{d(ON)} | Input current | | I _{IL} | -10 | _ | 60 | μΑ | V _{IN} = 0.8 V | 2 | |
| Total Color | | | I _{IH} | 50 | _ | 300 | μΑ | V _{IN} = 5.0 V | 2 | |
| Total Current Total Curre | Propagation delay time | | t _{d(ON)} | _ | _ | 50 | μs | I _O = 1 A | 2, 5 | |
| The following large The following large | | | t _r | _ | _ | 90 | μs | _ | 5 | |
| Open det. threshold current I _{OD} 2 10 100 μs 4, 5 Current limiter operating level I _{CS} 3.0 4.3 7.5 A 5 LVI operating level L.V.I — 5 6 V 3 Over voltage shut down Operating level OVSD 26 29 33 V 3 Output sustain voltage V _(SUS) — — — — — 25 V lout = 20 mA 5 Over Operating level OTSD 150 175 — °C 5 1 Hysteresis THYS — 15 — °C 5 1 Status on voltage V _{SL} — — 0.4 V I _S = 1 mA 4 | | | t _{d(OFF)} | _ | _ | 50 | μs | _ | 2, 5 | |
| Current limiter operating I cs 3.0 4.3 7.5 A 5 LVI operating level L.V.I — 5 6 V 3 Over voltage voltage level Operating level OVSD 26 29 33 V 3 Hysteresis VHYS 0.15 0.5 1.5 V 3 Output sustain voltage V _(sus) — — —25 V lout = 20 mA 5 Over temperature shut down Operating level OTSD 150 175 — °C 5 1 Hysteresis THYS — 15 — °C 5 1 Status on voltage V _{SL} — — 0.4 V I _S = 1 mA 4 | | | Tf | _ | _ | 50 | μs | _ | 5 | |
| LVI operating level L.V.I — 5 6 V 3 | | | I _{OD} | 2 | 10 | 100 | μs | | 4, 5 | |
| Over voltage shut down Operating level OVSD 26 29 33 V 3 Hysteresis VHYS 0.15 0.5 1.5 V 3 Output sustain voltage V _(SUS) — — -25 V lout = 20 mA 5 Over temperature shut down Operating level OTSD 150 175 — °C 5 1 Hysteresis THYS — 15 — °C 5 1 Status on voltage V _{SL} — — 0.4 V I _S = 1 mA 4 | - | | I _{CS} | 3.0 | 4.3 | 7.5 | Α | | 5 | |
| voltage shut down level Hysteresis VHYS 0.15 0.5 1.5 V 3 Output sustain voltage V _(SUS) — — — —25 V lout = 20 mA 5 Over temperature shut down Hysteresis THYS — 15 — °C 5 1 Status on voltage V _{SL} — — 0.4 V I _S = 1 mA 4 | LVI opera | ating level | L.V.I | _ | 5 | 6 | V | | 3 | |
| Output sustain voltage $V_{(SUS)}$ — — — — — — — $^{\circ}C$ | voltage shut | | OVSD | 26 | 29 | 33 | V | | 3 | |
| Over temperature shut down Operating level OTSD 150 175 — °C 5 1 Hysteresis THYS — 15 — °C 5 1 Status on voltage V _{SL} — — 0.4 V I _S = 1 mA 4 | | Hysteresis | VHYS | 0.15 | 0.5 | 1.5 | V | | 3 | |
| | Output sustain voltage | | $V_{(SUS)}$ | _ | _ | -25 | V | lout = 20 mA | 5 | |
| Status on voltage V_{SL} — 0.4 V $I_S = 1 \text{ mA}$ 4 | temper- ature shut | | | 150 | 175 | _ | °C | | 5 | 1 |
| | | Hysteresis | THYS | _ | 15 | _ | °C | | 5 | 1 |
| Status leakage current $I_{S(Leak)}$ -10 — 100 μA $V_s = 5.0 \text{ V}$ 4 | Status on voltage | | V _{SL} | _ | _ | 0.4 | V | I _S = 1 mA | 4 | |
| | Status leakage current | | S(Leak) | -10 | _ | 100 | μΑ | V _S = 5.0 V | 4 | |

Notes: 1. Design parameter only (no test)

Solenoid Drive Application and it's Waveform

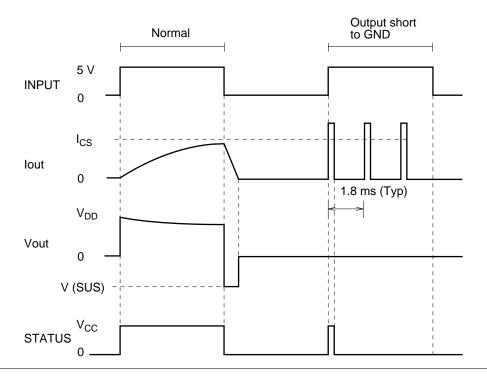


R1: Input series resistance to protect CMOS driver.

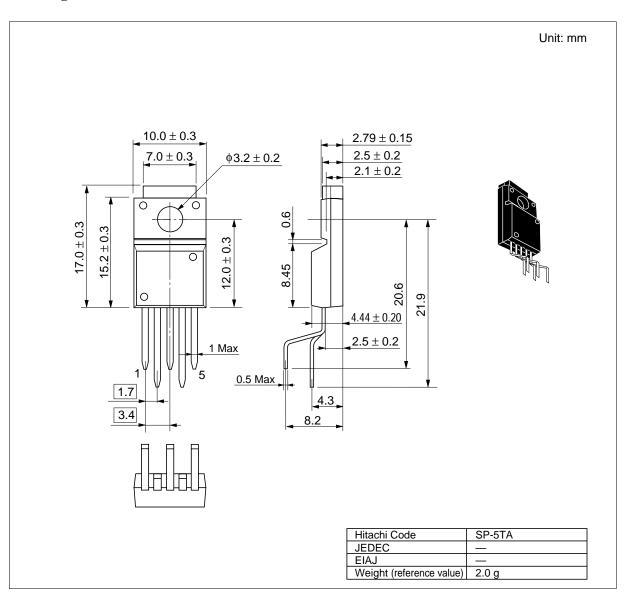
R2 : Pull up resistance at status output.

C1: The capacitor to compensate the inductance at $V_{\mbox{\scriptsize DD}}$ line.

D1, DZ1: for Reverse voltage clamp



Package Dimensions



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